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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,175	12/30/2003	Danh Dang	015114-069800US	5032

26059 7590 09/19/2006

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EXAMINER
TRIMMINGS, JOHN P

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 09/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,175	DANG ET AL.	
	Examiner	Art Unit	
	John P. Trimmings	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *8,13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-29 are presented for examination.

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign mentioned in the description (page 4): "system 100" in FIG. 1. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claim 8 is objected to because of the following informalities: line 6 of the claim cites, "... the interface connections ...", but in order to be both compatible with "the IP core" in the claim and compatible with the balance of the dependent claims, the examiner requests that the line be reworded to recite, "... ~~the~~ interface connections ...".. Appropriate correction is required.

3. Claim 8 is objected to because of the following informalities: line 8 of the claim should be corrected to recite, "... the set of test data ...".

4. Claim 13 is objected to because of the following informalities: line 4 of the claim should be corrected to recite, "... the set of test results ...".

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 8 recites the limitation "the set of functional blocks" in line 5. There is insufficient antecedent basis for this limitation in the claim.

6. Claim 8 recites the limitation "the IP core" in line 6. There is insufficient antecedent basis for this limitation in the claim.

7. Claim 8 recites the limitation "the reconfigurable device" in line 7. There is insufficient antecedent basis for this limitation in the claim.

8. Claim 8 recites the limitation "the reconfigurable device" in line 8. There is insufficient antecedent basis for this limitation in the claim.

9. Claim 9 recites the limitation "the IP core" in line 3. There is insufficient antecedent basis for this limitation in the claim.

10. Claim 10 recites the limitation "the IP core" in line 3. There is insufficient antecedent basis for this limitation in the claim.

11. Claim 10 recites the limitation "the IP core" in line 4. There is insufficient antecedent basis for this limitation in the claim.

12. Claim 12 recites the limitation "the IP core" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

13. Claim 15 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claim, as interpreted by the examiner, is drawn to a storage medium for storing a configuration of a device. The claim as such, is therefore non-statutory because "an information storage medium" is not a tangible object per se, because it is a broad limitation that may include a volatile device such as a RAM, as is mentioned in the applicant's disclosure. Also, the act of storing the

configuration of a device does not produce a tangible result. Where there is no physical transformation being claimed, a practical application would be established by a useful, concrete and tangible result. That result is useful if it has specific, substantial and credible utility. To satisfy section 101 requirements, the claim must be for a practical application of a Sec. 101 judicial exception, which can be identified in various ways:

. The claimed invention "transforms" an article or physical object to a different state or thing.

. The claimed invention otherwise produces a useful, concrete and tangible result.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

14. Claims 1-3, 8-10, 15-17 and 19-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Herron et al. (herein Herron), U.S. Patent No. 6996758.

As per claims 1 and 8:

Herron teaches a method for testing a set of interface connections in a reconfigurable device (see Title) between an IP core implementing at least one

specialized operation and a set of functional blocks (column 3 lines 34-40) adapted to implement general-purpose logic devices (see Abstract), the method comprising: creating a test program including a set of test data and a test configuration adapted to configure the set of functional blocks (column 1 lines 51-60 and column 2 lines 14-25) to implement a set of boundary scan registers (column 23 lines 30-32) connected with the interface connections of the IP core (see FIG. 27); configuring the reconfigurable device according to the test configuration (column 3 lines 57-67); inputting the test data into the reconfigurable device (for example, column 2 lines 58-67) to create a set of test results (column 3 lines 1-15); and analyzing the set of test results to determine the integrity of the set of interface connections (column 3 lines 34-40).

As per claims 2 and 9:

Herron further teaches the method of claim 1 or 8, wherein the set of boundary scan registers include a plurality of shift registers connected in series (column 15 lines 50-62), wherein each shift register is adapted to be connected with an interface connection of the IP core (column 15 lines 50-62 as applied to FIG. 27).

As per claims 3 and 10:

Herron further teaches the method of claim 2 or 9, wherein a first portion of the plurality of shift registers is adapted to be connected with a set of input interface connections of the IP core (FIG. 27 2702 and column 18 lines 14-20) and a second portion of the plurality of shift registers is adapted to be connected with a set of output interface connections (FIG. 27 2708 and column 18 lines 28-34) of the IP core (FIG. 27 2704 column 17 lines 65-67 and column 18 lines 1-13).

As per claim 15:

Herron teaches an information storage medium including a test configuration for configuring a reconfigurable device (see Abstract), the reconfigurable device having an IP core implementing at least one specialized operation and a set of functional blocks adapted to implement general-purpose logic devices (column 3 lines 34-40), the test configuration comprising a configuration of the set of functional blocks implementing a set of boundary scan registers (column 23 lines 30-32) connected with a set of interface connections of the IP core (see FIG. 27).

As per claim 16:

Herron further teaches the information storage medium of claim 15, wherein the set of boundary scan registers include a plurality of shift registers connected in series (column 15 lines 50-62), wherein each shift register is adapted to be connected with an interface connection of the IP core (column 15 lines 50-62 as applied to FIG. 27).

As per claim 17:

Herron further teaches the information storage medium of claim 16, wherein a first portion of the plurality of shift registers is adapted to be connected with a set of input interface connections of the IP core (FIG. 27 2702 and column 18 lines 14-20) and a second portion of the plurality of shift registers is adapted to be connected with a set of output interface connections (FIG. 27 2708 and column 18 lines 28-34) of the IP core (FIG. 27 2704 column 17 lines 65-67 and column 18 lines 1-13).

As per claim 19:

Herron further teaches the information storage medium of claim 15, further including a set of test data adapted to be input into the IP core via the set of functional blocks implementing the set of boundary scan registers (see Abstract).

As per claim 20:

Herron further teaches the information storage medium of claim 15, further including a set of expected test results (column 4 lines 24-32).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 4-7, 11-14 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herron et al. (herein Herron), U.S. Patent No. 6996758 as applied to claims 1, above, and further in view of Kiryu et al. (herein Kiryu), U.S. Patent Application Publication No. 2005/0138509.

As per claims 4, 11 and 18:

Where Herron fails to further teach, Kiryu discloses the method of claim 1 or 8 or 15, wherein the test configuration is defined with a hardware description language representation (see the Background of Kiryu). And in the Background, the advantage stated was that for scan chain testing used in design verification, testing a design within

scan chains, and verifying functionality of a design, is expedited with the use of HDL. One with ordinary skill in the art at the time of the invention, motivated as suggested, would have found it obvious to apply a modern test aid such as HDL as cited in Kiryu, in the design and test stages of a circuit using scan chains such as in Herron in order to test the device.

As per claims 5 and 12:

Kiryu further teaches the method of claim 4 or 11, wherein the creating a test program includes: combining the hardware description language representation of the test configuration with a hardware description language representation of the IP core to form a test hardware description; and analyzing the test hardware description to create a set of test data. Kiryu, in the Background describes such a process for both scan chains and the embedded logic. And in view of the motivation previously stated, the claims are rejected.

As per claims 6 and 13:

Herron further discloses the method of claim 5 or 12, wherein creating a test program further includes analyzing the test hardware description and the set of test data to create a set of expected test results; and wherein analyzing the test results includes comparing the set of test results with the set of expected test results (column 2 lines 58-67 and column 3 lines 1-3). And in view of the motivation previously stated, the claims are rejected.

As per claims 7 and 14:

Herron further suggests the method of claim 5 or 12, wherein analyzing the test hardware description is performed using automated test program generation software. The disclosure, in column 3 lines 16-26) states that during the test vector generation, "known test procedures" are applied in generating test vectors. Support for such a well known process in the art using ATPG may be found in analogous references such as by Renovell, "IS-FPGA: A New Symmetric FPGA Architecture with Implicit SCAN", November 1, 2001, IEEE International Test Conference 2001, page 930, column 2, 2nd paragraph. And in view of the motivation previously stated, the claims are rejected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John P Trimmings
Examiner
Art Unit 2138

jpt

GUY LAMARRE
PRIMARY EXAMINER